Abstract of the Disclosure

Disclosed is a method of manufacturing semiconductor devices, which can improve electrical characteristics of semiconductor devices. The method of manufacturing comprises the following steps of: forming a plurality of gates on a semiconductor substrate; forming an insulation layer on an entire surface of the semiconductor substrate to coat the plurality of gates; selectively removing the insulation layer by using a first mask pattern to form a contact hole, which exposes a source/drain junction and a conductive layer in a portion of the gates in the semiconductor substrate; removing the first mask pattern and forming a second mask pattern on the selectively removed insulation layer, the second mask pattern exposing the p+ source/drain junction in the semiconductor substrate; implanting ion into the p+ source/drain junction in the semiconductor substrate by using the second mask pattern as a mask; removing the second mask pattern and rapid thermal annealing the entire substrate in a activation temperature range of dopant which is implanted in the ion implantation step; and burying the contact hole with conductive material to form a bit line contact plug. The invention can effectively reduce bit line contact resistance but raise resistance uniformity without variation in related techniques such as etching and contact material for forming contacts.